connecting at least part of said first surface to said chip carrier via adhesive material.

17. (Amended) The method according to claim 11 wherein step etching comprises shielding at least part of said semiconductor unit and said carrier to prevent said etching from affecting the quality of said semiconductor unit and said carrier.

18. (Amended) The method according to claim 11 further comprising a step of electrically connecting said semiconductor unit to said chip carrier via said electrical connection device after etching.

19. (Amended) A method for reducing the size of at least a semiconductor unit in a process of packaging said semiconductor unit wherein said semiconductor unit includes a first surface, a second surface, and at least an electrical connection device located on said first surface, said method comprising the steps of:

dividing a wafer into a plurality of dice;

placing at least one die of said dice onto a seating apparatus, with said second surface exposed;

applying beams of light on said second surface to etch said dice, with said first surface shielded by said seating apparatus and thereby immunized against etching.

20. (Amended) The method according to claim 19 further comprising the steps of:

ending etching said die when the size of said die meets an expected specification;

moving said die from said seating apparatus to attach to a chip carrier in a way selected from among connecting said chip carrier via said first surface and connecting said chip carrier via said second surface according to the configuration of electrical connection between said die and said chip carrier.

REMARKS

1. Applicant appreciates the Examiner's thorough review of the present invention, and respectfully request reconsideration in light of the foregoing amendments and the following remarks.

2. Reconsideration and allowance of amended claims 1, 2, 3, 5, 9, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20 are respectfully requested in view of the foregoing amendments and the following remarks. Original claims 4, 6, 7, and 8 ultimately depend on amended claim 1, and original claim 13 ultimately depends on amended claim 11, and are therefore considered to be in condition for allowance.

Applicant respectfully traverses the rejection that claims 1-6, 8-12, 14-18 are unpatentable under 35 U.S.C. 103(a) over Dery et al. (U.S. Patent No. 6,074,895) in view of Hudak et al. (U.S. Patent No. 5,656,552). The claim amendments were made to further clarify distinctions between the claimed invention and the subject matter disclosed by Dery et al., Hudak et al., and Siniaguine (U.S. Patent No. 6,184,060).

Regarding the Examiner's rejection to claim 1, particularly the last 3 lines on page 2 and the first 3 lines on page 3 of the Office action, please note that what is shown in FIG. 1E of Dery et al. is a chip package completed as a result of applying some of the steps shown in FIGS. 1A-1D of Dery et al., and what is shown in FIG. 2D of Dery et al. is a chip package completed as a result of applying some of the steps shown in FIGS. 2A-2C of Dery et al., and the surface 111a instead of another part of the IC chip 110 (110 is not a surface but is the entire IC chip) is chemically modified by plasma 116. In FIG. 1A (and col 3, lines 58-67) of Dery et al., IC chip 110 is placed on an electrically driven electrode 132, and plasma 116 is applied onto its passivation surface 111a (having electrical connection device such as bump 114 thereon, and corresponding to the first surface 22 of semiconductor unit 25 in the present invention as shown in FIGS. 1-5) to chemically modify the passivation surface 111a. FIG. 1B (and column 4, lines 37-39) of Dery et al. shows a step of mechanically roughening the surface 124 of chip carrier 120. FIG. 1C (and column 4, lines 39-40) of Dery et al. shows a step of treating the surface 124 of chip carrier by plasma 116. After being treated by the step shown in FIG. 1A, IC chip 110 of Dery et al. is integrated with the chip carrier 120 which may have been treated by the step shown either in FIG. 1B or in FIG. 1C, thereby the package shown in FIG. 1E of Dery et al. is achieved by finally applying encapsulant 140 (column 5, lines 9-10). In FIGS. 2A-2C (and col 5, lines 23-55) of Dery et al., IC chip 210 is joined to chip carrier 220, and then the joined IC chip 210 and chip carrier 220 are placed on electrically driven electrode 232, in order to apply plasma 216 onto the surface 224 of chip carrier 220 and the passivation layer 211 of IC chip 210. It can thus be seen the part of IC chip 110 or 210 being modified by plasma 116 or 216 according to Dery et al. is the passivation surface 111a or passivation layer 211. Either the passivation surface 111a or the passivation layer 211 corresponds to the surface 22 of semiconductor unit 25 in the present invention, as can be understood from FIGS. 1-5 of the present invention. Because plasma 116 (or 216) must be applied onto the part (surface 111a or layer 211 or surface 224 of Dery et al.) having bumps 114 or 214 (electrical connection device) thereon or facing bump 214, Dery et al. requires a plasma chamber 130 to restrict the flowing freedom of plasma 116 or 216, and requires an electrically driven electrode 132 or 232 to conduct the plasma to the entire surface 111a or surface 224, so that the plasma application can be feasible. Regarding lines 16-18 on page 3 of the Office action, please note that

the object of Dery et al. is to modify surfaces of IC chip and chip carrier so that the adhesion between encapsulant and the IC chip, and between encapsulant and the chip carrier can be improved (column 2, lines 56-64). Dery et al. does not disclose any suggestion of reducing the size of the semiconductor unit by plasma etching.

According to the present invention, it is the surface 23 instead of surface 22 from which the semiconductor unit 25 is etched to reduce the size of the semiconductor unit 25, and it is the chip carrier 21 that acts as a seating apparatus on one hand when etching the semiconductor unit 25 from surface 23, while functions on the other hand as an essential part of the IC package to be made (FIG. 6 of the present invention). The present invention differs from the art of Dery et al. in the fact that its object is to reduce the thickness of a semiconductor unit by an etching process, and the etching process is carried out from a second surface (23 in FIGS. 1-5 of the present invention), which is back-to-back relative to a first surface (22 in FIGS. 1-5 of the present invention) having electrical connection device 24 thereon and corresponding to the surface 111a or 211 in the art of Dery et al.

Furthermore, in claim 1 of the present invention, attaching occurs such that the chip carrier (21 in FIGS. 1-6) acts as a seating apparatus when etching the semiconductor unit and functions as an essential part of the package to be made (FIG. 6). The advantage achieved by the attaching step of the present invention is unprecedented. To applicant's best knowledge, no prior art has ever suggested integrating a semiconductor unit with a carrier to provide the advantage that the carrier acts on one hand as a seating apparatus for the semiconductor unit to be etched for reducing its size, and functions on the other hand as a chip carrier for an IC package to be made. Please note that that in FIG. 2C of Dery et al., the electrode 232 instead of chip carrier 220 acts as a seating apparatus for the chip carrier 220 and the IC chip 210 to have the surface 224 and the passivation layer 211 thereof treated by plasma. The IC chip 110 (FIG. 1A) and/or the chip carrier 220 (FIG. 2C) are placed on an electrically driven electrode 132 or 232 which is part of an etching equipment, not part of the package to be made.

Although Hudak et al. mentioned thinning a die (or a wafer) by reactive ion etching, chemical etching, or mechanical grinding, its step (2 in FIG. 1) of thinning a die (or a wafer) is completed before testing the die (or the wafer), and before integrating the die (or the wafer) with a carrier, i.e., before bonding the die to a flat substrate indicated by step 4 of FIG. 1. The process of thinning a wafer in the art of Hudak et al. is shown in FIG. 11, wherein the thinned wafer is removed from handle-wafer and is bonded to a chip carrier (flat substrate) after being tested (FIG. 1). Claims 1 and 11 of the present invention differs from the art of Hudak et al. in the fact that the semiconductor unit in the present invention is attached to a carrier in such a way that the semiconductor unit is seated on the carrier for

etching one of its surfaces, with the carrier acting not only as a seating apparatus but also as an essential part of the IC package to be made. There is no need of separating the semiconductor unit and the carrier after completing the etching. Furthermore, Hudak et al. does not suggest attaching (connecting) the semiconductor unit and the carrier by means of electrical connection device such as bump. In spite of the fact that the advantages of the claimed invention resulting from the differences are significant, no prior art, to applicant's best knowledge, has ever suggested a scheme providing the advantages even though the art of Hudak et al. was disclosed more than 4 years ago.

As can be seen from the above remarks, the object of the present invention is different from that of the art of Dery et al., the way the present invention achieves its object is different from that of the art of Hudak et al., and the advantages achieved by the present invention are unprecedented. It cannot be obvious to those of ordinary skill in the art to think of combining the arts of Dery et al. and Hudak et al. to provide the methods of claims 1 and 11 of the present invention, and to provide the advantages achieved by the present invention. Accordingly, the amended claims 1 and 11 overcome the obviousness rejection based on Dery et al. and Hudak et al.

Regarding the Examiner's rejection (Office action page 4, lines 6-8) to claims 6 and 8, please note that the encapsulant 140 or 240 (FIG. 1E or FIG. 2D) in the art of Dery et al. is not used for preventing the IC chip 110 (or 210) and carrier 120 (or 220) from being etched, instead it is applied (column 4, lines 21-32; column 5, lines 55-58), after the surface 111a (or 211a) of passivation layer 111 (or 211) and the surface 124 (or 224) of carrier 120 (or 220) have been chemically modified, to the integrated IC chip and carrier to fill the space formed between surface 111a (or 211a) of passivation layer 111 (or 211) and surface 124 (or 224) of chip carrier 120 or 220 by bumps 114 or 214. In the art of Dery et al., plasma etching is to chemically modify the surface 111a (or 211a) of passivation layer 111 (or 211) and the surface 124 (or 224) of carrier 120 (or 220), so that both the surface 111a (or 211a) and the surface 124 can provide improved adhesion for encapsulant 140 or 240 to better fill the space formed between the surface 111a (or 211a) and the surface 124 (or 224) by bumps 114 or 214. If encapsulant 140 or 240 is used to prevent the IC chip 110 (or 210) and carrier 120 (or 220) from being etched by plasma, it would also prevent the surface 111a (or 211a) of passivation layer 111 (or 211) and the surface 124 (or 224) of carrier 120 (or 220) from being chemically modified by plasma, contradicting the object of Dery et al.

Regarding the Examiner's rejection (Office action page 4, lines 15-17) to claim 15, please note that the surface 111a of passivation layer 111 of IC chip 110 and the surface 124 of carrier 120 face each other, with bumps 114 or 214 (electrical connection devices) therebetween. If the surface 111a of passivation layer 111 of IC chip 110 is prevented by carrier/seating apparatus from being etched, it would

also be prevented by carrier/seating apparatus from being chemically modified, and nothing would be done to improve its adhesion for encapsulant to fill the space formed between it and the surface 124 by bumps, contradicting the object of Dery et al.

Regarding the Examiner's rejection (Office action page 5, lines 5-6) to claim 18, please note that a flip-chip on board assembly/package is very different from a lead-on-chip package.

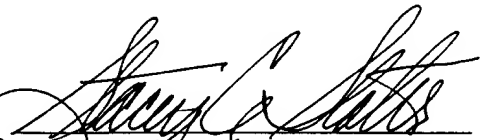
Claim 11 of the present invention has been so amended that the claimed method is limited to making a lead-on-chip package. The limitation added to claim 11 and those added to the claims depending on claim 11 can be supported by lines 12-25 on page 8 of the present application. The amendment of claim 11 were made to further clarify distinctions between the claimed invention and the subject matter disclosed by Dery et al., Hudak et al., and Siniaguine (U.S. Patent No. 6,184,060). To applicant's best knowledge, no any prior art has ever suggested applying etching process in reducing the size of a semiconductor unit when making a lead-on-chip package.

Responding to the Examiner's rejection (Office action pages 6-7) to claim 19, claim 19 of the present invention has been amended to limit etching means to applying beams of light. The limitation added to claim 19 and those added to claim 20 can be supported by lines 26-28 on page 8, page 9, and lines 1-2 on page 10 of the present application. To applicant's best knowledge, no prior art has ever suggested applying beams of light in achieving the same object.

Accordingly, the amended claims 1, 11, and 19 overcome the obviousness rejection based on Dery et al., Hudak et al., and Siniaguine, and are in condition for allowance and such actions are respectfully requested. Claims 2-10 depend on the amended claim 1, claims 12-18 depend on the amended claim 11, and claim 20 depends on the amended claim 19, all are therefore in condition for allowance and such actions are also respectfully requested.

Respectfully submitted,

KLARQUIST SPARKMAN, LLP

By 
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Marked-up Version of Amended Claims
Pursuant to 37 C.F.R. §§ 1.121

1. (Amended) A method for reducing the size of at least a semiconductor unit in a process of [packaging] making a package including a carrier and said semiconductor unit, said semiconductor unit including a first surface and a second surface, said method comprising the steps of:

[(A)] attaching at least a part of [a] said first surface [of said semiconductor unit] to [a] said carrier; and

[(B)] etching said semiconductor unit from [a] said second surface [of said semiconductor unit] until the size of said semiconductor unit meets an expected specification.

2. (Amended) The method according to claim 1 wherein said semiconductor unit is etched by [means selected from among using gas and] using beams of light.

3. (Amended) The method according to claim 1 wherein said semiconductor unit is etched by means selected from among using gas and using plasma.

5. (Amended) The method according to claim [4] 1 wherein said [specified range is the range spanning between 2 mil and 6 mil] semiconductor unit is attached to said carrier according to a configuration of bump connection.

9. (Amended) The method according to claim 1 wherein said semiconductor unit is attached to said carrier according to a configuration [selected from among bump connection and lead-on chip] of lead-on-chip packaging.

10. (Amended) The method according to claim 1 wherein said carrier is [selected from among a chip tray and] a chip carrier, [and] said semiconductor unit includes at least an electrical connection device located on said first surface, and attaching includes a connecting said electrical connection device to said chip carrier.

11. (Amended) A method for reducing the size of at least a semiconductor unit in a process of lead-on-chip packaging [said semiconductor unit] wherein said semiconductor unit includes a first surface, a second surface, and at least an electrical connection device located on said first surface, said method comprising the steps of:

[(A)] attaching said semiconductor unit to a [seating apparatus] chip carrier in such a way that said semiconductor unit and said chip carrier are in a configuration of lead-on-chip, with said first surface facing said [seating apparatus] chip carrier and said second surface exposed; and

[(B)] etching said semiconductor unit from said second surface until the size of said semiconductor unit meets an expected specification.

12. (Amended) The method according to claim 11 wherein [said semiconductor unit is etched by means selected from among using gas, beams of light, and plasma] etching includes applying beams of light on said second surface .

14. (Amended) The method according to claim 11 wherein [said seating apparatus is selected from among a chip tray, and a chip carrier connectible with said semiconductor unit; and wherein] said expected specification means that the thickness of said semiconductor unit measured relative to said first surface is within a specified range.

15. (Amended) The method according to claim 11 wherein said [first surface is prevented by said seating apparatus from being etched] configuration of lead-on-chip means that part of said first surface is connectible with said chip carrier via adhesive material and said semiconductor unit is electrically connectible with said chip carrier via said electrical connection device.

16. (Amended) The method according to claim 11 [further comprising a step of moving said semiconductor unit from said seating apparatus to a chip carrier with said second surface attaching to said chip carrier via adhesive material] wherein attaching includes a step of connecting at least part of said first surface to said chip carrier via adhesive material.

17. (Amended) The method according to claim 11 [further comprising a step of moving said semiconductor unit from said seating apparatus to a carrier with said first surface attaching to said carrier via at least a bump] wherein step etching comprises shielding at least part of said semiconductor unit and said carrier to prevent said etching from affecting the quality of said semiconductor unit and said carrier.

18. (Amended) The method according to claim [11] 16 further comprising a step of [moving said semiconductor unit from said seating apparatus to a chip carrier for forming a lead-on chip package]

electrically connecting said semiconductor unit to said chip carrier via said electrical connection device after etching.

19. (Amended) A method for reducing the size of at least a semiconductor unit in a process of packaging said semiconductor unit wherein said semiconductor unit includes a first surface, a second surface, and at least an electrical connection device located on said first surface, said method comprising the steps of:

dividing a wafer into a plurality of dice;

placing at least one die of said dice onto a seating apparatus, with said second surface exposed;

[etching said die from] applying beams of light on said second surface to etch said dice, with said first surface shielded by said seating apparatus and thereby immunized against etching[;].

[ending etching said die when the size of said die meets a predetermined specification, and moving said die from said seating apparatus to a chip carrier.]

20. (Amended) The method according to claim 19 [wherein said seating apparatus includes a tray which said first surface is in, said predetermined specification means that the thickness of said die measured relative to said first surface is within a predetermined range, and when said die is moved to said chip carrier, said die attaches to said chip carrier] further comprising the steps of:

ending etching said die when the size of said die meets an expected specification;

moving said die from said seating apparatus to attach to a chip carrier in a way selected from among connecting said chip carrier via said first surface and connecting said chip carrier via said second surface according to the [type] configuration of electrical connection between said die and said chip carrier.